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CLAIMS:

1. A pulse width limiting circuit, comprising:
a clock signal correction block configured to receive a
conditioned clock pulse and generate a corrected clock output
5 signal, wherein the clock signal comprises a train of clock
pulses, each of which has a rising clock edge, a falling clock
edge and a variable width;
a block delay module configured to accept an
unconditioned clock signal and introduce a specified pulse
10 width delay, wherein the block delay module comprises a
plurality of delay sub-blocks of fixed delay; and
a high low clock pulse shuttle circuit configured to
accept the conditioned clock signal output, wherein the high
low clock pulse shuttle comprises a first field effect
15 transistor (FET) coupled to the correction block and a second
FET coupled to a conditioned clock signal output interconnect.
2. The system of claim 1, wherein the unconditioned clock
input is coupled to the source of a positive FET in the high
20 low clock pulse shuttle.
3. The system of claim 1, where a correction block circuit
further comprises a correction unit and a leak detector unit,
wherein the correction block is employed to transmit the clock
25 pulse to the high low clock pulse shuttle.
4. The system of claim 2, wherein the high low clock pulse
shuttle is coupled to an interconnect, wherein the
interconnect is employed to convey an unmodified clock pulse.

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5. The system of claim 1, further comprising a node to transmit the clock pulse between stages of a delay sub-block.
6. The system of claim 1, further comprising a node to transmit the conditioned clock pulse between the delay sub-block and the correction block.
7. The system of claim 1, further comprising a node to transmit the conditioned clock pulse between the correction block, the clock shuttle and clock pulse inverter.
8. The system of claim 3, further comprising a leak detector calculating a voltage potential between two digital devices.
9. The system of claim 7, wherein an uncorrected clock pulse bypasses the correction block and the clock shuttle for delivery through the clock pulse output inverter.
10. A method for performing a plurality of clock pulse widths limiting in clock pulses, comprising:
initiating a clock in pulse as a result of a clock cycle;
routing a clock pulse;
initiating a correction block;
determining a voltage leak;
forwarding a clock pulse through a clock shuttle node;
injecting a clock pulse through a block delay module;
sequentially advancing a clock pulse through delay sub-blocks;
disconnecting and resetting individual delay sub-blocks;
altering a clock pulse that is greater than a predetermined pulse width; and

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substantially passing through a clock pulse less than or equal to a predetermined pulse width.

11. The method of claim 11, wherein a clock pulse width is
5 selected for correction by a specific state within a correction block.

12. The method of claim 11, wherein a clock pulse width is
10 deselected for correction by a specific state within a correction block.

13. The method of claim 11, wherein a selected clock pulse is
passed through a clock pulse correction block and checked by a
leak detector.

14. The method of claim 11, wherein a deselected clock pulse
15 is passed through a clock shuttle and output through a clock pulse inverter.

15. The method of claim 11, wherein a selected clock pulse is
20 passed through a clock pulse correction block, checked by a leak detector, and input to a block delay module.

16. The method of claim 11, wherein the block delay module is
25 conditioning the clock pulse using a series of delay sub-blocks.

17. The method of claim 11, wherein the delay sub-blocks are
30 sequentially disconnecting and resetting as the clock pulse is passing.

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18. The method of claim 11, wherein the conditioned clock pulse is output to the correction block.

19. The method of claim 11, wherein a completely conditioned
5 clock pulse outputs to a conditioned clock pulse dependent device.

20. A computer program product for authenticating code in a computer system, the computer program product having a medium
10 with a computer program embodied thereon, the computer program comprising:

computer code for determining undesirable clock pulse width;

15 computer code for forwarding undesired clock pulses to a correction block;

computer code for desired clock pulses to bypass the pulse width correction and go directly to the device output; and

20 computer code for incrementing a sequential delay for cascading a series of delay sub-blocks.

21. A computer program for providing desirable clock pulse widths in a computer system, the clock pulse correction device including a computer program comprising:

25 computer code for determining undesirable clock pulse width;

computer code for forwarding undesired clock pulses to a correction block;

30 computer code for bypassing the correction block, sending desired clock pulses directly to the device output; and

computer code for incrementing a sequential delay for cascading a series of delay sub-blocks.